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EXAMINER	
AMRANY, ADI	

ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,216	OKADA ET AL.	
	Examiner	Art Unit	
	Adi Amrany	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicants' arguments filed April 28, 2006 have been fully considered but they are not persuasive. Applicants maintain that Tominaga does not describe or suggest the limitations of the claims. These statements, however, are not presented with any supporting arguments or reasoning to convince the examiner that the limitations are not anticipated by the references.

Tominaga discloses a structure that corresponds to an "abnormality signal output means for outputting an abnormality signal to the power source circuits when an abnormality occurs in the own circuit." This structure was presented in the rejection of claim 1 (Tominaga, figure 2, item 34; column 5, lines 56-68; column 6, lines 1-13). Applicants did not rebut the examiner's contention that these limitations were met, except to state that the references does not describe or suggest such a structure. The AC input monitoring circuit (34) monitors the AC power input, and in the event of an abnormality, outputs a signal to the operation monitoring circuits (38) of the other power source circuits.

Applicants' argument that Tominaga does not describe or suggest that the inverters (power source circuits) have a structural arrangement in which an output voltage is monitored to thereby stably control the output voltage to a desired voltage is also not persuasive. Tominaga discloses a voltage stabilizer (figure 2, item 35). Further, Luo, also discloses a monitoring structural arrangement (figure 3A, items 12, 14), as will be discussed below.

Applicants further contend that Luo does not supplement the deficiencies or drawback in the teachings of Tominaga, in failing to fully meet the limitations of the claimed invention. This statement, however, does not specifically rebut the relevance and use of Luo in the §103 obviousness rejections made in the non-final rejection.

Claims 1-2 and 4 were not amended, and therefor, remain rejection under 35 U.S.C. §102(b) over Tominaga. Claims 5, 10, and 12 were amended to include the limitations of "a drive circuit that generates a switching signal for controlling an output voltage" and "a voltage monitoring circuit that monitors the output voltage thereby to control the switching signal generated from the drive circuit whereby the output voltage is stably controlled to a desired voltage." These elements, as will be discussed below, as taught by Tominaga, and alternatively, by Luo. Thus, claims 5-6, and 8-16 remain rejected under §102(b) over Tominaga, and, alternatively, claims 3 and 5-16 are rejected under 35 U.S.C. §103 as being obvious over Tominaga, in view of Luo. Claims 3 and 7 were originally rejected under §103 over Tominaga, in view of Luo. The rejections are presented below.

Claim Objections

2. Claim 10 is objected to because portions of the claim appear to be written twice. Namely, lines 7-15 of claim 10 appear on the bottom of page 20 and again at the top of page 21 of applicants' response, filed April 28, 2006.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-6, and 8-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Tominaga (US 5,237,208).

With respect to claim 1, Tominaga discloses a multiple output power source apparatus (figure 1) comprising:

a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9) equipped with independent output control circuits (figure 2, and column 5, lines 22-26),

wherein the power source circuits equipped with independent output control circuits respectively comprises: abnormality signal output means (figure 2, item 34, and column 6, lines 1-13) for conducting operation shutdown of own circuit (column 5, lines 56-68) when an abnormality occurs in the own circuit and for outputting an abnormality signal to other power source circuits (column 6, lines 9-13).

With respect to claim 2, Tominaga discloses the multiple output power source apparatus according to claim 1, and further discloses an abnormality signal input means (figure 3, column 6, lines 14-22, and column 6, line 46 to column 7, line 5) for inputting the abnormality signal outputted from other power source circuit, and operation

shutdown means (figure 3, and column 7, lines 6-29) for conducting the operation shutdown of the own circuit by the input of the abnormality signal by the abnormality signal input means.

With respect to claim 4, Tominaga discloses the multiple output power source apparatus according to claim 2, and further discloses the operation of a power source circuit selected from the plurality of power source circuits equipped with the independent output control circuits is continued by the independent output control circuit even when the abnormality signal has been outputted from the other power source circuits (column 6, lines 56-61). The power source circuits can be set to shut down when any combination of other power source circuits fail. This includes keeping a power source circuit active even though any number of other power source circuits have failed.

With respect to claim 5, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9) equipped with independent output control circuits (figure 2, and column 5, lines 22-26), wherein the power source circuits comprise:

synchronous oscillation signal output means (column 7, lines 33-42) for outputting a synchronous oscillation signal synchronized with the switching oscillation frequency of own circuit to output control circuits of other power source circuits;

a drive circuit (figure 2, item 35; figure 6, items 351-353; column 5, lines 46-49) that generates a switching signal for controlling an output voltage; and

a voltage monitoring circuit (figure 2, item 35; figure 6, items 351-353; column 5, lines 46-49)

With respect to claim 6, Tominaga discloses the multiple output power source apparatus according to claim 5, and further discloses a synchronous oscillation signal input means (figure 4, and column 7, lines 43-48) for inputting a synchronous oscillation signal outputted from the other power source circuit, and control means (column 7, lines 49-58) for conducting synchronous control of a switching oscillation frequency used in output control of the own circuit by inputting the synchronous oscillation signal by the synchronous oscillation signal input means.

With respect to claim 8, Tominaga discloses the multiple output power source apparatus according to claim 6, and further discloses the operation of a power source circuit selected from the plurality of power source circuits is continued (column 6, line 46 to column 7, line 5, namely column 6, lines 56-61) by the independent output control circuit even when the abnormality signal has been outputted from the other power source circuits. A power source circuits can be kept active even though any number of other power source circuits have failed, as discussed above.

With respect to claim 9, Tominaga discloses the multiple output power source apparatus according to claim 6, and further discloses a control means (column 7, lines 43-55) for synchronously controlling a switching phase used for output control of the own circuit by a switching phase of the synchronous oscillation signal by the synchronous oscillation signal input means.

With respect to claim 10, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9), wherein;

at least two of the plurality of power source circuits are connected by a synchronous line (figure 2, item 20, and column 5, lines 22-26),

first and second power source circuits connected by the synchronous line comprise independent control circuits (figure 2, and column 5, lines 22-26), respectively,

the control circuit provided in the first power source circuit comprises:

synchronous signal output means (column 7, lines 33-42) for outputting a synchronous signal synchronized with the switching frequency of own circuit to the synchronous line;

abnormality signal output means (figure 2, item 34, and column 6, lines 9-13) for outputting an abnormity signal indicating the abnormality occurrence in the own circuit to the synchronous line;

the control circuit provided in the second power source circuit comprises:

synchronous signal input means (column 7, lines 43-55) for inputting the synchronous signal outputted to the synchronous line into the own circuit;

abnormality signal input means (column 6, lines 14-23) for inputting the abnormality signal outputted to the synchronous line into the own circuit;

a drive circuit (figure 2, item 35; figure 6, items 351-353; column 5, lines 46-49) that generates a switching signal for controlling an output voltage; and

a voltage monitoring circuit (figure 2, item 35; figure 6, items 351-353; column 5, lines 46-49)

With respect to claim 11, Tominaga discloses the multiple output power source apparatus according to claim 10, and further discloses

the control circuit provided in the first power source circuit further comprises abnormality signal input means (column 7, lines 1-5) for inputting the abnormality signal outputted to the synchronous line into the own circuit,

the control circuit provided in the second power source circuit further comprises abnormality signal output means (column 6, lines 46-68) for outputting the abnormality signal indicating the abnormality occurrence in the own circuit to the synchronous line, and

the first and second power source circuits shut down (column 7, lines 6-29) the own circuits when the abnormality signal has been inputted form the synchronous line.

With respect to claim 12, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9), wherein;

at least two of the plurality of power source circuits are connected by a synchronous line (figure 2, item 20, and column 5, lines 22-26),

first and second power source circuits connected by the synchronous line comprise independent control circuits (figure 2, and column 5, lines 22-26),

the control circuits provided in the first and second power source circuits respectively comprise:

frequency synchronization means (figure 2, item 27, and column 5, lines 50-56, and column 7, lines 43-58) for controlling switching frequency of own circuit by using a synchronous signal outputting to the synchronous line;

abnormality signal detection means (column 8, lines 29-34) for detecting the abnormality signal outputted to the synchronous line and shutting down the own circuit;

a drive circuit (figure 2, item 35; figure 6, items 351-353; column 5, lines 46-49) that generates a switching signal for controlling an output voltage; and

a voltage monitoring circuit (figure 2, item 35; figure 6, items 351-353; column 5, lines 46-49)

With respect to claim 13, Tominaga discloses the multiple output power source apparatus according to claim 12, and further discloses;

the synchronous signal comprises a clock signal (column 5, lines 49-55) of a predetermined frequency,

the abnormality signal is generated by changing the clock signal (column 8, lines 5-34, namely lines 29-34),

the abnormality signal detection means detects change of the clock signal (column 5, lines 56-63).

With respect to claim 14, Tominaga discloses the multiple output power source apparatus according to claim 13, and further discloses the change of the clock signal is generated by the first power source circuit and/or second power source circuit (column 8, lines 5-34, namely lines 18-23).

With respect to claim 15, Tominaga discloses the multiple output power source apparatus according to claim 13, and further discloses the change of the clock signal is implemented by stopping the clock signal (column 6, line 62 to column 7, line 5), and the abnormality signal detection manes measures an interval during which the clock signal is stopped and shuts down the own circuit when it is detected that the stop state continues for a predetermined interval or longer (column 7, lines 23-29). Tominaga discloses that AND circuits output a control signal to the mode control circuit. This control signal is "0" or "off" when any number of the detection output signals from the power supply circuits are abnormal. An abnormal signal includes the absence of a signal, which would occur when the oscillator is stopped.

With respect to claim 16, Tominaga discloses the multiple output power source apparatus according to claim 13, and further discloses the change of the clock signal is implemented by changing a voltage level of the clock signal (column 8, lines 18-23) and the abnormality signal detection means measures the voltage level of the clock signal

(column 8, lines 29-34) and shuts down (column 8, lines 32-34, release of failure signal "F") the own circuit when a predetermined voltage level is detected. Tominaga discloses that the outputs of the oscillators are passed through an AND circuit. The AND circuit detects any deviation among the plurality of oscillating signals and if one is detected outputs a parallel release signal. A deviation includes a change in voltage, a change in frequency, or any change that will trigger the AND circuit.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 5-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tominaga, in view of Luo (US 2005/0073783).

With respect to claim 3, Tominaga discloses the multiple output power source apparatus according to claims 1 and 2, as discussed in the 102(b) rejection above.

Tominaga does not expressly discloses that the abnormality signal output means and the abnormality signal input means conduct input and output of the abnormality signal by using a single terminal.

Luo discloses a multiple output power source (figure 1) comprising a plurality of power source circuits (figure 1, items 10, 101-10N, and paragraph 32, lines 1-3) equipped with independent output control circuits (figures 3A and 3B, and paragraph

38), wherein the abnormality signal output means and the abnormality input means conduct input and output of the abnormality signal by using a single terminal (figure 1, "comm line" 23 connects to each power source circuit at a single terminal, and paragraph 36).

Tominaga and Luo are analogous art because they are from the same field of endeavor, namely parallel power systems.

At the time of the invention by applicant it would have been obvious to a person of ordinary skill in the art to combine the input monitoring circuit and operation mode monitoring circuit disclosed in Tominaga with the single communication terminal disclosed in Luo.

The motivation for doing so would have been to reduce the number of terminals on the power sources and to reduce the length of transmission wire required to transmit the abnormality signal.

With respect to claim 5, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9) equipped with independent output control circuits (figure 2, and column 5, lines 22-26), wherein the power source circuits comprise synchronous oscillation signal output means (column 7, lines 33-42) for outputting a synchronous oscillation signal synchronized with the switching oscillation frequency of own circuit to output control circuits of other power source circuits.

Luo discloses:

a drive circuit (figure 3A, item 12; paragraph 38, lines 3-7) that generates a switching signal for controlling an output voltage; and

a voltage monitoring circuit (figure 3A, item 14; paragraph 38, lines 3-7; paragraph 71, lines 6-19; paragraph 77, lines 1-6).

Luo and Tominaga are analogous as discussed above. At the time of the invention by applicants, it would have been obvious to combine the multiple output power source apparatus disclosed in Tominaga with the drive circuit and voltage monitoring circuit disclosed in Luo. The motivation for doing so would have been to protect the power source apparatus from damage resulting from an excessive voltage output.

With respect to claim 6, Tominaga and Luo disclose the multiple output power source apparatus according to claim 5, and Tominaga further discloses a synchronous oscillation signal input means (figure 4, and column 7, lines 43-48) for inputting a synchronous oscillation signal outputted from the other power source circuit, and control means (column 7, lines 49-58) for conducting synchronous control of a switching oscillation frequency used in output control of the own circuit by inputting the synchronous oscillation signal by the synchronous oscillation signal input means.

With respect to claim 7, Tominaga and Luo disclose the multiple output power source apparatus according to claims 6.

Luo discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 10, 101-10N, and paragraph 32, lines 1-3) equipped with independent output control circuits (figures 3A and 3B, and

paragraph 38), wherein the synchronous oscillation signal out means and the synchronous oscillation input means conduct input and output by using a single terminal (figure 1, "sync" line connects to each power source circuit at a single terminal, and paragraph 35).

Tominaga and Luo are analogous art because they are from the same field of endeavor, namely parallel power systems.

At the time of the invention by applicant it would have been obvious to a person of ordinary skill in the art to combine the AC synchronizing signal disclosed in Tominaga with the single clock terminal disclosed in Luo.

The motivation for doing so would have been to reduce the number of terminals on the power sources and to reduce the length of transmission wire required to transmit the synchronizing signal.

With respect to claim 8, Tominaga and Luo disclose the multiple output power source apparatus according to claim 6, and Tominaga further discloses the operation of a power source circuit selected from the plurality of power source circuits is continued (column 6, line 46 to column 7, line 5, namely column 6, lines 56-61) by the independent output control circuit even when the abnormality signal has been outputted from the other power source circuits. A power source circuits can be kept active even though any number of other power source circuits have failed, as discussed above.

With respect to claim 9, Tominaga and Luo disclose the multiple output power source apparatus according to claim 6, and Tominaga further discloses a control means (column 7, lines 43-55) for synchronously controlling a switching phase used for output

control of the own circuit by a switching phase of the synchronous oscillation signal by the synchronous oscillation signal input means.

With respect to claim 10, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9), wherein;

at least two of the plurality of power source circuits are connected by a synchronous line (figure 2, item 20, and column 5, lines 22-26),

first and second power source circuits connected by the synchronous line comprise independent control circuits (figure 2, and column 5, lines 22-26), respectively,

the control circuit provided in the first power source circuit comprises:

synchronous signal output means (column 7, lines 33-42) for outputting a synchronous signal synchronized with the switching frequency of own circuit to the synchronous line,

abnormality signal output means (figure 2, item 34, and column 6, lines 9-13) for outputting an abnormity signal indicating the abnormality occurrence in the own circuit to the synchronous line,

the control circuit provided in the second power source circuit comprises:

synchronous signal input means (column 7, lines 43-55) for inputting the synchronous signal outputted to the synchronous line into the own circuit, and

abnormality signal input means (column 6, lines 14-23) for inputting the abnormality signal outputted to the synchronous line into the own circuit.

Luo discloses:

a drive circuit (figure 3A, item 12; paragraph 38, lines 3-7) that generates a switching signal for controlling an output voltage; and

a voltage monitoring circuit (figure 3A, item 14; paragraph 38, lines 3-7; paragraph 71, lines 6-19; paragraph 77, lines 1-6).

With respect to claim 11, Tominaga and Luo disclose the multiple output power source apparatus according to claim 10, and Tominaga further discloses

the control circuit provided in the first power source circuit further comprises abnormality signal input means (column 7, lines 1-5) for inputting the abnormality signal outputted to the synchronous line into the own circuit,

the control circuit provided in the second power source circuit further comprises abnormality signal output means (column 6, lines 46-68) for outputting the abnormality signal indicating the abnormality occurrence in the own circuit to the synchronous line, and

the first and second power source circuits shut down (column 7, lines 6-29) the own circuits when the abnormality signal has been inputted form the synchronous line.

With respect to claim 12, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9), wherein;

at least two of the plurality of power source circuits are connected by a synchronous line (figure 2, item 20, and column 5, lines 22-26),

first and second power source circuits connected by the synchronous line comprise independent control circuits (figure 2, and column 5, lines 22-26),

the control circuits provided in the first and second power source circuits respectively comprise:

frequency synchronization means (figure 2, item 27, and column 5, lines 50-56, and column 7, lines 43-58) for controlling switching frequency of own circuit by using a synchronous signal outputting to the synchronous line, and

abnormality signal detection means (column 8, lines 29-34) for detecting the abnormality signal outputted to the synchronous line and shutting down the own circuit.

Luo discloses:

a drive circuit (figure 3A, item 12; paragraph 38, lines 3-7) that generates a switching signal for controlling an output voltage; and

a voltage monitoring circuit (figure 3A, item 14; paragraph 38, lines 3-7; paragraph 71, lines 6-19; paragraph 77, lines 1-6).

With respect to claim 13, Tominaga and Luo disclose the multiple output power source apparatus according to claim 12, and Tominaga further discloses;

the synchronous signal comprises a clock signal (column 5, lines 49-55) of a predetermined frequency,

the abnormality signal is generated by changing the clock signal (column 8, lines 5-34, namely lines 29-34),

the abnormality signal detection means detects change of the clock signal (column 5, lines 56-63).

With respect to claim 14, Tominaga and Luo disclose the multiple output power source apparatus according to claim 13, and Tominaga further discloses the change of the clock signal is generated by the first power source circuit and/or second power source circuit (column 8, lines 5-34, namely lines 18-23).

With respect to claim 15, Tominaga and Luo disclose the multiple output power source apparatus according to claim 13, and Tominaga further discloses the change of the clock signal is implemented by stopping the clock signal (column 6, line 62 to column 7, line 5), and the abnormality signal detection manes measures an interval during which the clock signal is stopped and shuts down the own circuit when it is detected that the stop state continues for a predetermined interval or longer (column 7, lines 23-29). Tominaga discloses that AND circuits output a control signal to the mode control circuit. This control signal is "0" or "off" when any number of the detection output signals from the power supply circuits are abnormal. An abnormal signal includes the absence of a signal, which would occur when the oscillator is stopped.

With respect to claim 16, Tominaga and Luo disclose the multiple output power source apparatus according to claim 13, and Tominaga further discloses the change of the clock signal is implemented by changing a voltage level of the clock signal (column 8, lines 18-23) and the abnormality signal detection means measures the voltage level of the clock signal (column 8, lines 29-34) and shuts down (column 8, lines 32-34, release of failure signal "F") the own circuit when a predetermined voltage level is detected. Tominaga discloses that the outputs of the oscillators are passed through an AND circuit. The AND circuit detects any deviation among the plurality of oscillating signals and if one is detected outputs a parallel release signal. A deviation includes a change in voltage, a change in frequency, or any change that will trigger the AND circuit.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Bretz (US 6,894,468) discloses a parallel power system comprising a drive circuit and voltage output monitor circuit (figure 2, items 204, 205; column 6, lines 33-47).

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adi Amrany whose telephone number is (571) 272-0415. The examiner can normally be reached on weekdays, from 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AA

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